In this example, the photocells of the first row (photocells PC1_1 and PC1_2) are processed first. Thereafter, the photocells in the second row (photocells PC2_1 and PC2_2) are processed. During the processing of the photocells of the first row, the following steps may be performed. First, all the photocells in the first row are sampled. The sampled values are then held by the sample circuit for each respective column. The photocells in the first row are then reset. Then, each photocell in the first row is converted one photocell at a time (i.e., in a time sequential manner) by the amplifier. For example, the photocell PC1_1 in the first column is first converted by the amplifier and then the photocell PC1_2 in the second column is converted by the amplifier.

During the processing of the photocells of the second row, the following steps may be performed. First, all the photocells in the second row are sampled. The sampled values are then held by the sample circuit for each respective column. The photocells in the second row are then reset. Then, each photocell in the second row is converted one photocell at a time (i.e., in a time sequential manner) by the amplifier. For example, the photocell PC2_1 in the first column is first converted by the amplifier and then the photocell PC2_2 in the second column is converted by the amplifier.

During the reading of the first row, the READ_1 signal is asserted so that the voltage (V_{light}) of the photo cells in the first row are provided to the respective sample circuit (e.g., capacitors). As described earlier, there is a sample circuit for each column in the array.

It is noted that both sample signals are asserted during the sampling of the V_{light} for the first row. When the first photo cell of the first row is being converted, the first sample signal 560 is asserted, while the second sample signal 570 is not asserted. When the amplifier is being reset, both the first sample signal 560 and the second sample signal 570 are not asserted. When the second photo cell of the first row is being converted, the second sample signal 570 is asserted, while the first sample signal 560 is not asserted.

Similarly, both sample signals are asserted during the sampling of the V_{light} for the second row. When the first photo cell of the second row is being converted, the first sample signal 560 is asserted, while the second sample signal 570 is not asserted. When the amplifier is being reset, both the first sample signal 560 and the second sample signal 570

are not asserted. When the second photo cell of the second row is being converted, the second sample signal 570 is asserted, while the first sample signal 560 is not asserted.

Both output voltages (Vlight and Vreset) are needed for processing each photocell. Specifically, the difference of these two voltages (Vlight and Vreset) is proportional to the light that is received during the integration time of the pixel. The read signal (e.g., READ1 and READ2) places the buffered version of the voltage at Vlight of each photocell of a respective row onto an associated column when the buffer is biased with the column current source. The reset signal (e.g., RESET1 and RESET2) recharges the Vlight node of each photocell of a respective row to the reset voltage. This signal can be lowered after the row is converted and provide a rolling shutter function or it can be held high until a common start of conversion is commenced, and then all the reset signals are released.

FIG. 7 illustrates a diagram that illustrates exemplary circuits that may be coupled to the amplifier of FIG. 2 for gain manipulation and level shifting. A first mechanism 710 (e.g., a VSHIFT voltage and switch circuit elements) may be coupled to the first input 132 and the output 134 of the amplifier 130 for performing level shifting of the output of the amplifier 130. The first mechanism 710 can include a second mechanism (e.g., capacitor and switch circuit elements) that is coupled to the first input and the output of the amplifier for performing gain manipulation of the amplifier 130.

For example, the voltage (VSHIFT) may be employed to modify or set the zero difference of the amplifier. A plurality of different integration capacitors (e.g., CINT_1, CINT_2, .., CINT_N) that may have different capacitor values are provided to affect the gain of the amplifier 130. A switch 720 is provided to utilize the first and second mechanisms for level shifting and gain manipulation.

One advantage of the architecture is that a single amplifier is employed for multiple columns instead of an amplifier for each column used by the prior art approaches. By reducing the number of components in the design, the present invention reduces costs, saves power for cordless applications, and reduces silicon area.

Another advantage of the read out architecture of the present invention is that since a single amplifier is utilized across columns, gain matching from column to column, which can be a difficult, time-consuming, and costly process, is obviated.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.
